ABSTRACT

A computer system is disclosed having a bus capability determination mechanism. In a preferred embodiment, the computer system includes a backplane having sockets into which system and peripheral boards may be inserted. The sockets are coupled together by a backplane bus that includes a bus capability line. Each board preferably includes a voting circuit that, when enabled, limits the voltage on the capability signal line to no more than a predetermined voltage that is indicative of the capability of the board. The voltage on the capability signal line will thus be determined by the board having the lowest voltage limit. The clock source for the bus can then be set to the clock rate indicated by the voltage on the capability signal line. Zener devices are preferably used to carry out the voting operation, and may be disabled after the voting operation is complete.

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